PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference SC12600ET	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/EP2004/006481	International filing date *(day/month/year)* 16.06.2004	Priority date *(day/month/year)* 17.06.2003
International Patent Classification (IPC) or national classification and IPC H03L7/093, H03H7/01		
Applicant FREESCALE SEMICONDUCTORS, INC		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 5 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 2 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
20.01.2005	16.03.2005
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Waters, D Telephone No. +49 89 2399-6937

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/EP2004/006481

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages	
1, 3-9	as originally filed
2	received on 26.01.2005 with letter of 19.01.2005
Claims, Numbers	
1-5	received on 26.01.2005 with letter of 19.01.2005
Drawings, Sheets	
1/2-2/2	as originally filed

☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☒ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☒ the claims, Nos. 6
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/EP2004/006481

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-5
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-5
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-5
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Re Item V

Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Of the documents cited in the International Search Report the following are mentioned in this communication:

D1: US-A-5 774 023 (IRWIN JAMES STUART) 30 June 1998 (1998-06-30)

D2: US-A-5 424 689 (GILLIG STEVEN F ET AL) 13 June 1995 (1995-06-13)

D3: CRANINCKX J ET AL: "FULLY INTEGRATED CMOS DCS-1800 FREQUENCY SYNTHESISER" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 33, no. 12, December 1998 (1998-12), pages 2054-2065, XP000880509 ISSN: 0018-9200

1. The claimed subject matter is new and involves an inventive step according to Article 33 (2) and (3) PCT as explained below.

1.1 As discussed in the Written Opinion of 20th of October 2004 and acknowledged in the applicants' letter of 19th of January 2005, figure 4 of document discloses a similar circuit to that of claim 1. The applicants argue in their letter of 19th of January 2005 that the PLL filter of amended claim 1 is distinguished over this prior art by the following features:

a) it comprises only 3 capacitors and 2 resistors;

b) it is 'suitable for integration onto an integrated circuit'.

The feature 'small capacitor values' discussed in the applicants' letter of 19th of January 2005 does not appear in the amended claims.

1.2 Regarding a) above, if claim 1 is interpreted as defining a PLL filter comprising exactly 3 capacitors and 2 resistors and no more (see 3. below) then this feature appears novel against the disclosure of D1. Furthermore whilst it may be argued that there is a general drive in the electronics industry to miniaturise and reduce component count, no incentive is found in D1 to alter the filter circuit to the specific one defined by amended claim 1, which is therefore considered inventive.

1.3 Regarding b) in 2.1 above, since the components of the PLL filter of D1 could be

integrated onto an integrated circuit board the feature is considered neither new nor inventive.

2. Since dependent claims 2-5 contain all of the features of claim 1 they are likewise considered to be new and inventive.

3. For information (in case the applicants are considering entering the regional phase), the wording of claim 1 is inconsistent since the phrase 'comprises only...' followed later by '...and further comprising...' reads as if the 'comprising only' applies just to the words as far as '...and further comprising...'.

CLAIMS

1. A phase locked loop system for integration onto an integrated circuit comprising a charge pump (12) arranged to output a first current over a first charge pump path while a second current is output over a second charge pump path; and a phase locked loop filter (13) characterised in that it comprises only a first capacitor (C2) electrically coupled between the first charge pump path and the second charge pump path; and a parallel resistor/capacitor circuit (23) electrically coupled to the second charge pump path with the resistor/capacitor circuit (23) having a second capacitor (C1) and a first resistive element (R1); wherein the first capacitor (C2) and second capacitor (C1) are connected in series to allow a voltage associated with the first capacitor (C2) and a voltage associated with the parallel resistor/capacitor circuit (23) to be added together, and further comprising an extra pole having a second resistive element (R2) and a shunt capacitor (C3) coupled, at one end to the second resistive element (R2) and at the other end to a reference voltage.

2. A phase locked loop system according to claim 1, wherein the current flow in the second path is greater than the current flow in the first path to allow a decrease in the capacitance of the phase locked loop filter (13).

3. A phase locked loop system according to any preceding claim, wherein the added voltage is arranged to control a voltage controlled oscillator (13).

4. An electronic device incorporating a phase locked loop system according to any preceding claim.

5. A radiotelephone incorporating a phase locked loop system according to any preceding claim.

Another example of a dual path PLL filter was proposed by Koo, IEEE Journal of Solid-State Circuit, Vol. 37, No. 5, May 2002 in which a dual path PLL filter incorporated a single active device, an amplifier.

However, the use of active devices within a PLL filter increases both phase noise and power consumption as well as increasing the complexity of the PLL filter.

US 5,774,023 discloses a loop filter that includes a high current first pole filter capacitor, a high current first pole damping resistor, a low current first pole filter capacitor, a low current first pole damping resistor and a first pole filter capacitor in which the loop filter is driven by a first charge pump output when current pulses from the charge pump are commensurate with a final narrow loop bandwidth otherwise the loop filter is driven by a second charge pump output. As such US 5,774,023 discloses the switching of current source between the first charge pump output and the second charge pump output rather than simultaneous output.

According to an aspect of the present invention there is provided a phase locked loop filter according to claim 1.

This provides the advantage of allowing a loop filter to be integrated onto a single chip using only three capacitors and two resistive elements without requiring the use of an active component, for example a voltage adder or an integrator.

An embodiment of the invention will now be described, by way of example, with reference to the drawings, of which:

Figure 1 illustrates a phase locked loop incorporating a filter according to an embodiment of the present invention;